FIG. 1

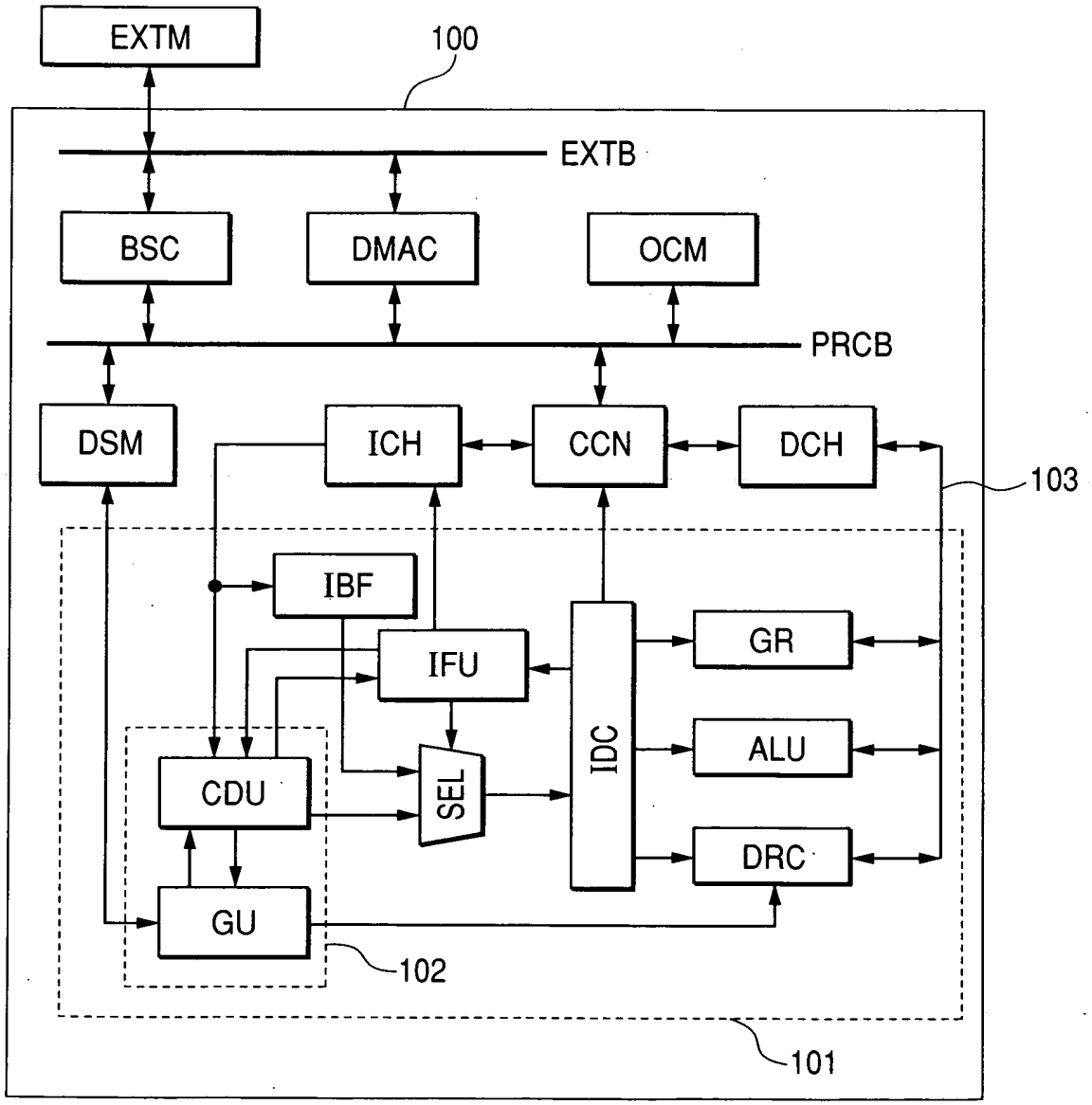

EXTM
100
EXTB
BSC
DMAC
OCM
PRCB
DSM
ICH
CCN
DCH
103
IBF
IFU
GR
ALU
DRC
IDC
SEL
CDU
GU
102
101

FIG. 2

LOOP FREQUENCY	OPERATION OF DRC CONTROL UNIT 102	SOFTWARE TO BE EXECUTED
FIRST TIME	TEMPORARY DECISION	NORMAL SW
SECOND TIME	NORMAL SW ACQUISITION FINAL DECISION	NORMAL SW
THIRD TIME	DRC RECONFIGURATION	NORMAL SW
FOURTH TIME		DRC DRIVER SW
FIFTH-n-TH TIME		DRC DRIVER SW

FIG. 3

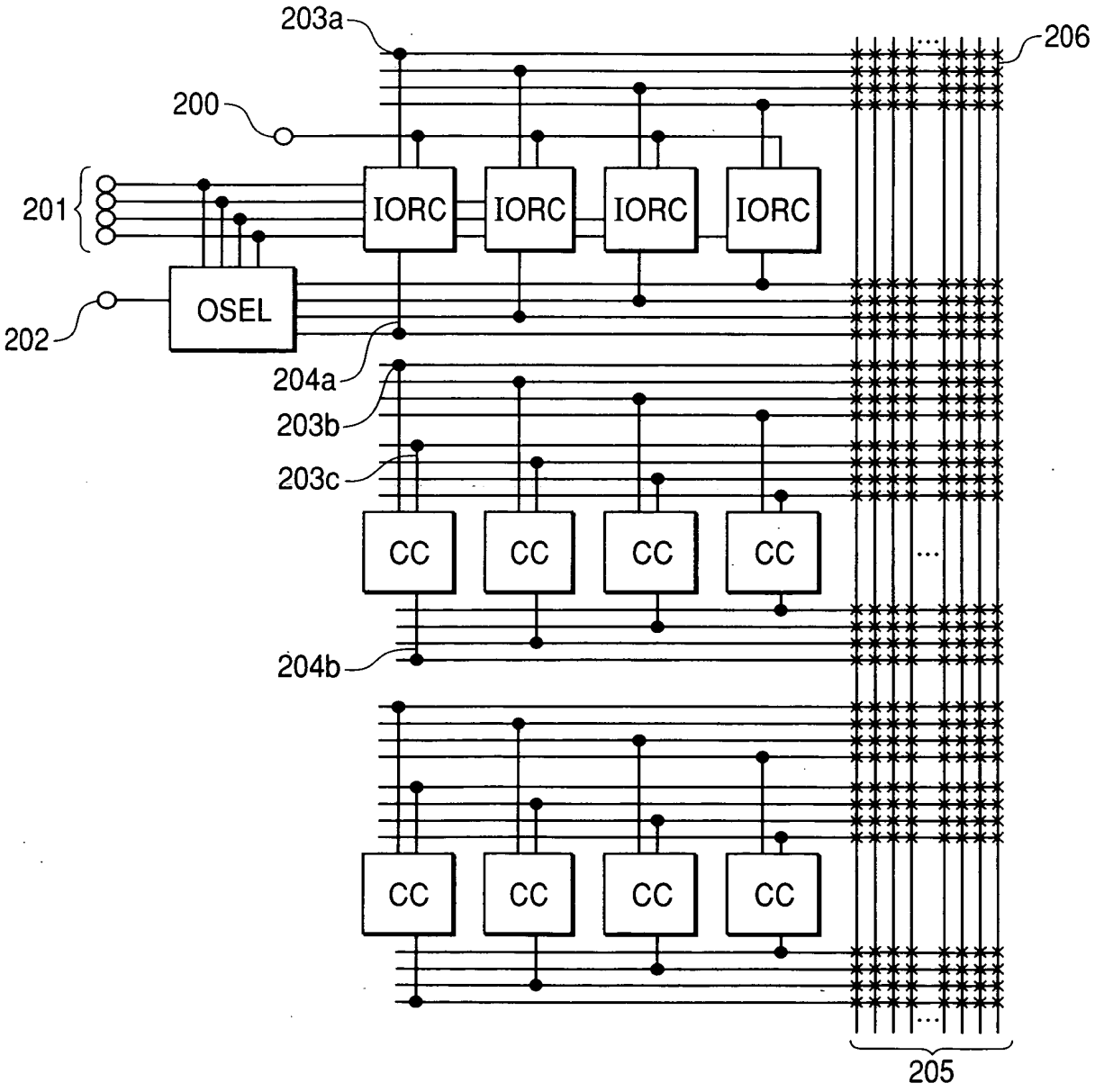

203a
206
200
201
IORC
IORC
IORC
IORC
OSEL
202
204a
203b
203c
CC
CC
CC
CC
204b
CC
CC
CC
CC
205

FIG. 4

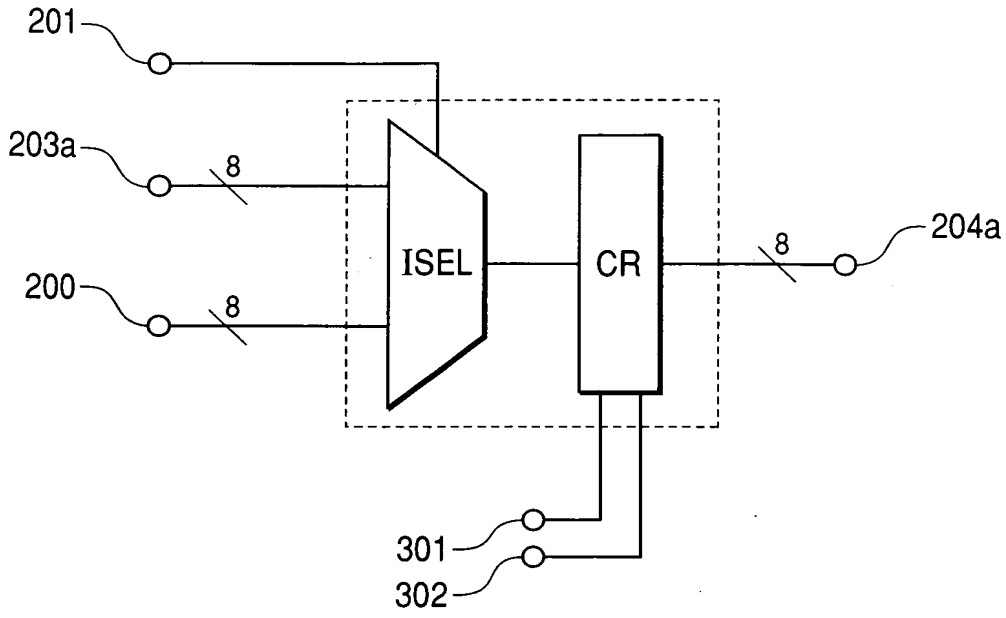

201
203a
8
200
8
ISEL
CR
8
204a
301
302

FIG. 5

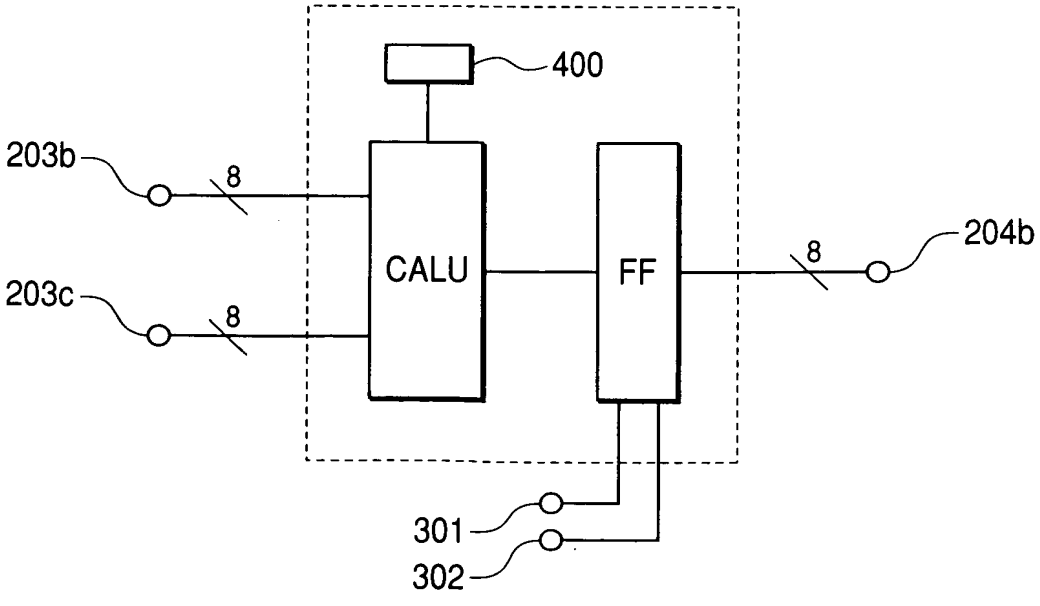

400
203b
8
203c
8
CALU
FF
8
204b
301
302

FIG. 6

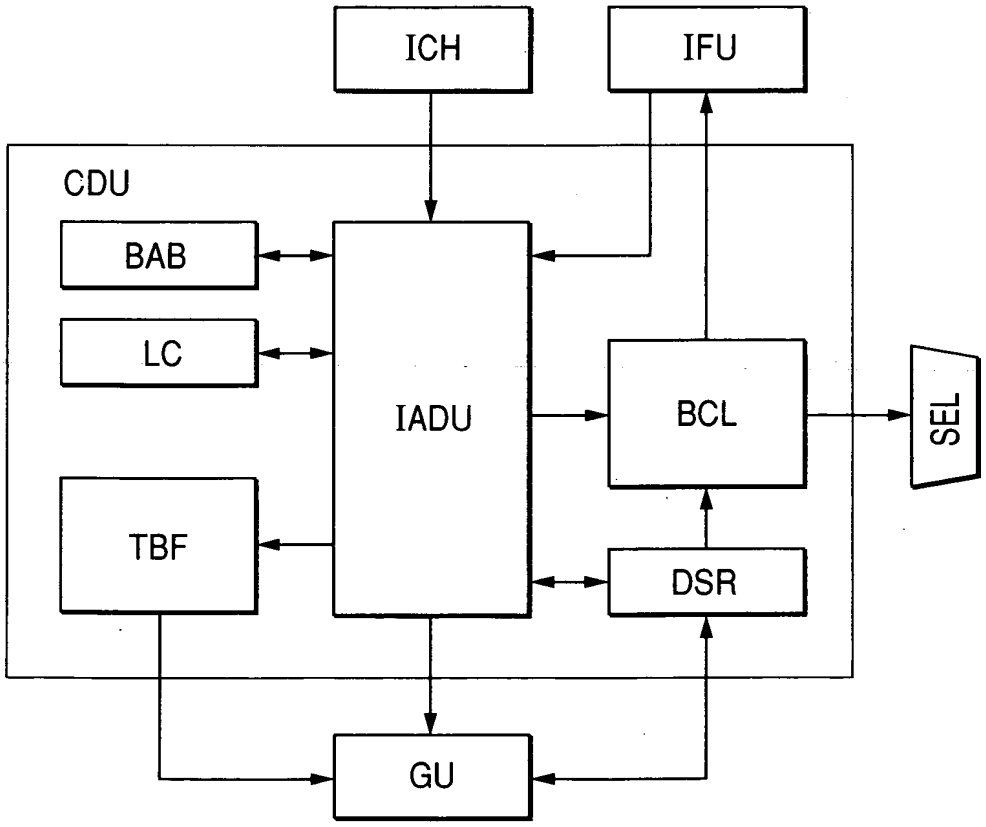


FIG. 7

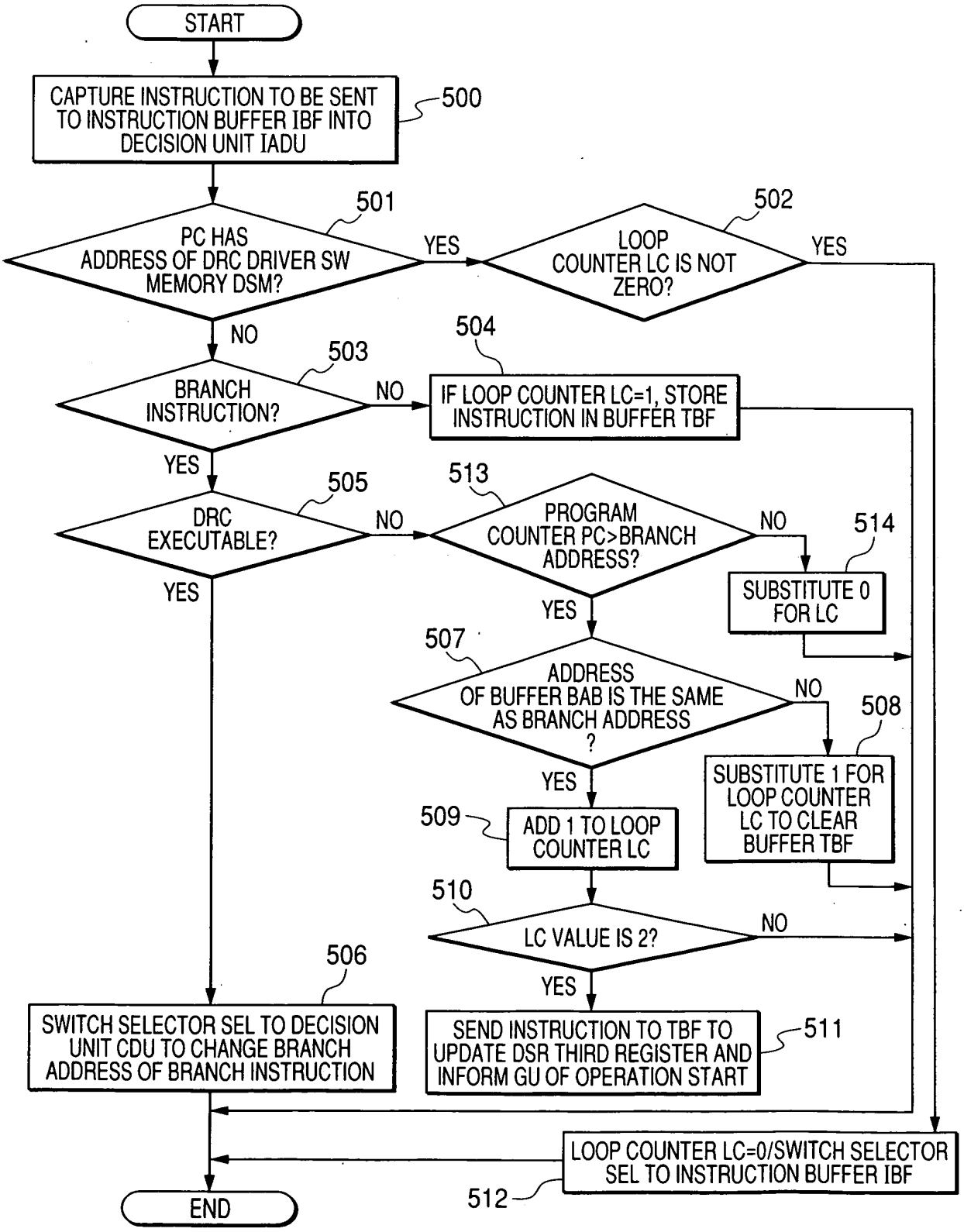

START
CAPTURE INSTRUCTION TO BE SENT TO INSTRUCTION BUFFER IBF INTO DECISION UNIT IADU
500
PC HAS ADDRESS OF DRC DRIVER SW MEMORY DSM?
501
YES
LOOP COUNTER LC IS NOT ZERO?
502
YES
NO
BRANCH INSTRUCTION?
503
NO
IF LOOP COUNTER LC=1, STORE INSTRUCTION IN BUFFER TBF
504
YES
DRC EXECUTABLE?
505
NO
PROGRAM COUNTER PC>BRANCH ADDRESS?
513
NO
SUBSTITUTE 0 FOR LC
514
YES
YES
ADDRESS OF BUFFER BAB IS THE SAME AS BRANCH ADDRESS ?
507
NO
SUBSTITUTE 1 FOR LOOP COUNTER LC TO CLEAR BUFFER TBF
508
YES
ADD 1 TO LOOP COUNTER LC
509
LC VALUE IS 2?
510
NO
YES
SWITCH SELECTOR SEL TO DECISION UNIT CDU TO CHANGE BRANCH ADDRESS OF BRANCH INSTRUCTION
506
SEND INSTRUCTION TO TBF TO UPDATE DSR THIRD REGISTER AND INFORM GU OF OPERATION START
511
LOOP COUNTER LC=0/SWITCH SELECTOR SEL TO INSTRUCTION BUFFER IBF
512
END

FIG. 8

(A)

```
1   L001:
2     STS     MACL,@-R15
3     MOV     #8,R0
4   L002:
5     DT      R0
6     MOV     @R6,R3
7     MOV     @R5,R2
8     MUL     R3,R2
9     MOV     @R4,R1
10    STS     MACL,R7
11    SUB     R7,R1
12    MOV     R1,@R5
13    MOV     @R4,R3
14    ADD     R3,R7
15    MOV     R7,@R4
16    ADD     #4,R4
17    ADD     #4,R5
18    BF      L002
19  L003:
20    NOP
21    LDS     @R15+,MACL
22    RTS
23    NOP
```

(B)

```
1   L002:
2     DT      R0
3     MOV     @R6,R3
4     MOV     @R5,R2
5     MUL     R3,R2
6     MOV     @R4,R1
7     STS     MACL,R7
8     SUB     R7,R1
9     MOV     R1,@R5
10    MOV     @R4,R3
11    ADD     R3,R7
12    MOV     R7,@R4
13    ADD     #4,R4
14    ADD     #4,R5
15    BF      L002
```

(C)

```
1     MOV     R6,dR6
2     MOV     R5,dR5
3     MOV     R4,dR4
4   L002a:
5     MOV     @dR6,dR3
6     MOV     @dR5,dR2
7     MOV     @dR4,dR1
8     DT      R0
9     MOV     dR1,@dR5
10    MOV     dR7,@dR4
11    NOP
12    BF      L002a
13    MOV     dR5,R5
14    MOV     dR4,R4
15    JMP     L003
```

(D)

MOV	DATA TRANSFER INSTRUCTION
ADD	ADDITION INSTRUCTION
SUB	SUBTRACTION INSTRUCTION
MUL	MULTIPLICATION INSTRUCTION
DT	DECREMENT+BRANCH SET INSTRUCTION
BF	BRANCH INSTRUCTION
JMP	NONBRANCH INSTRUCTION
NOP	NO OPERATION
LDS	SYSTEM REGISTER LOAD
STS	SYSTEM REGISTER STORE
RTS	RETURN INSTRUCTION
R*	GENERAL REGISTER*
dR*	IORC*

FIG. 9

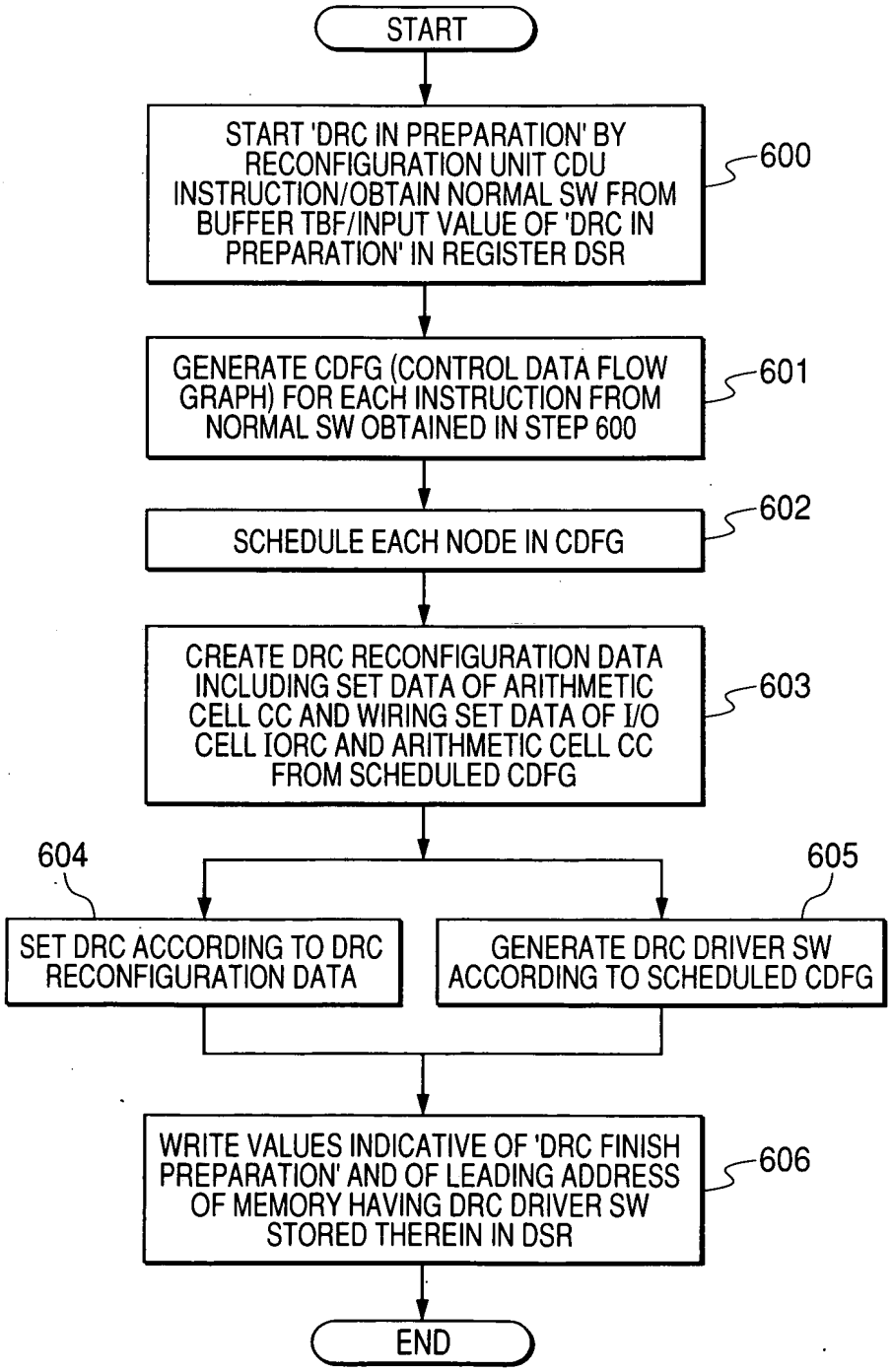

START
START 'DRC IN PREPARATION' BY RECONFIGURATION UNIT CDU INSTRUCTION/OBTAIN NORMAL SW FROM BUFFER TBF/INPUT VALUE OF 'DRC IN PREPARATION' IN REGISTER DSR
600
GENERATE CDFG (CONTROL DATA FLOW GRAPH) FOR EACH INSTRUCTION FROM NORMAL SW OBTAINED IN STEP 600
601
SCHEDULE EACH NODE IN CDFG
602
CREATE DRC RECONFIGURATION DATA INCLUDING SET DATA OF ARITHMETIC CELL CC AND WIRING SET DATA OF I/O CELL IORC AND ARITHMETIC CELL CC FROM SCHEDULED CDFG
603
604
605
SET DRC ACCORDING TO DRC RECONFIGURATION DATA
GENERATE DRC DRIVER SW ACCORDING TO SCHEDULED CDFG
WRITE VALUES INDICATIVE OF 'DRC FINISH PREPARATION' AND OF LEADING ADDRESS OF MEMORY HAVING DRC DRIVER SW STORED THEREIN IN DSR
606
END

FIG. 10

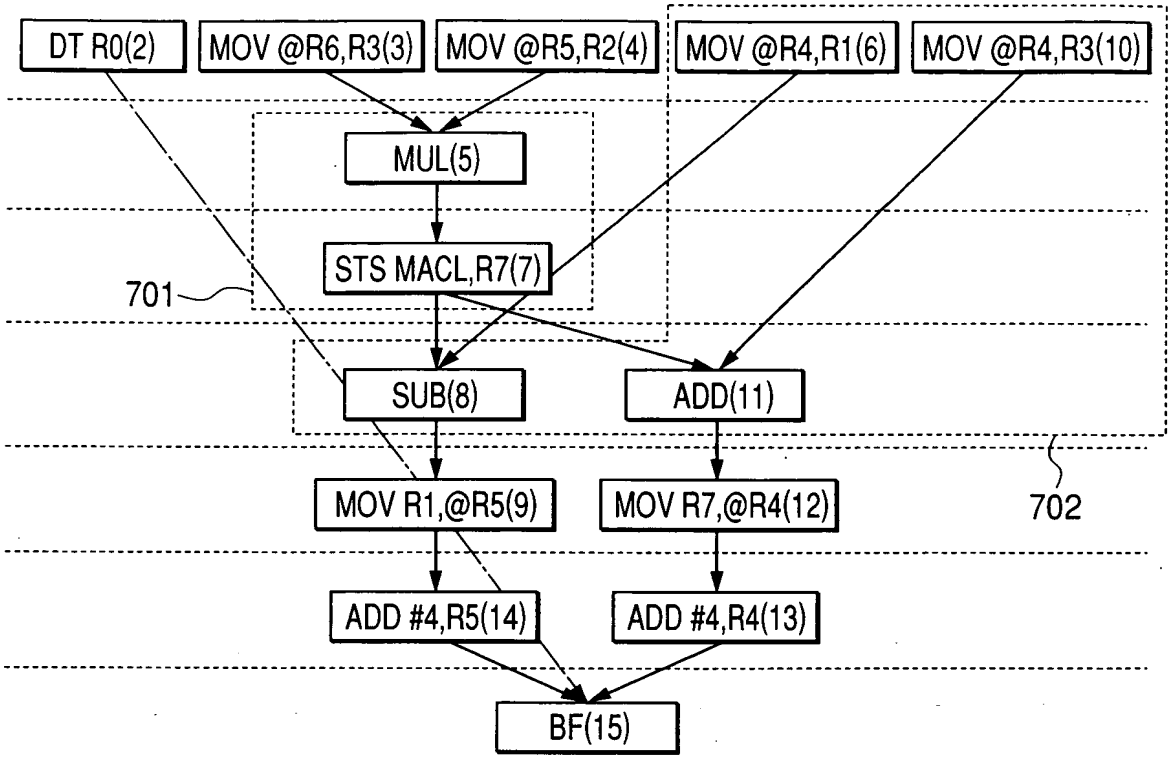

DT R0(2)
MOV @R6,R3(3)
MOV @R5,R2(4)
MOV @R4,R1(6)
MOV @R4,R3(10)
MUL(5)
STS MACL,R7(7)
701
SUB(8)
ADD(11)
MOV R1,@R5(9)
MOV R7,@R4(12)
702
ADD #4,R5(14)
ADD #4,R4(13)
BF(15)

FIG. 11

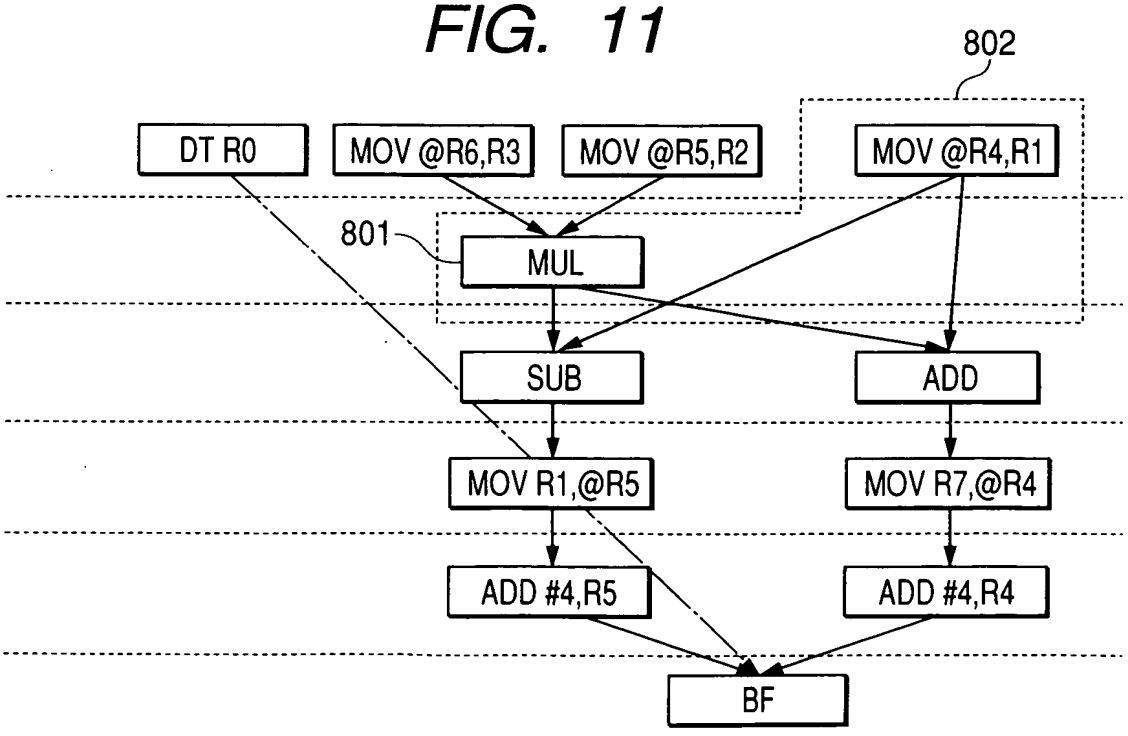

802
DT R0
MOV @R6,R3
MOV @R5,R2
MOV @R4,R1
801
MUL
SUB
ADD
MOV R1,@R5
MOV R7,@R4
ADD #4,R5
ADD #4,R4
BF

FIG. 12

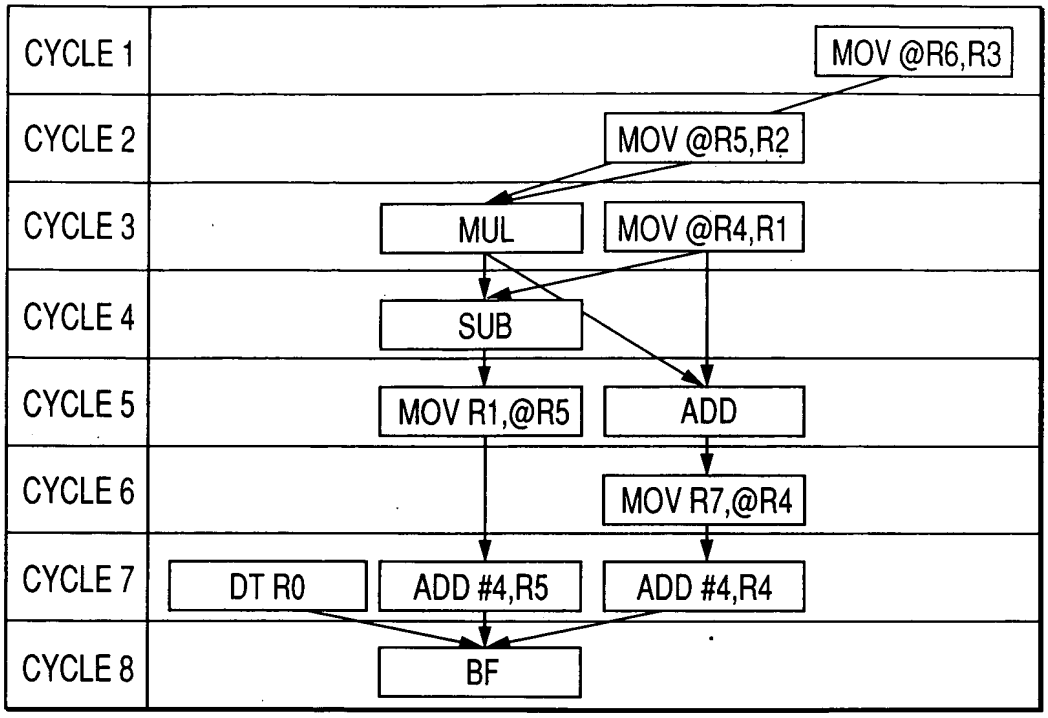

CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
CYCLE 5
CYCLE 6
CYCLE 7
CYCLE 8
MOV @R6,R3
MOV @R5,R2
MUL
MOV @R4,R1
SUB
MOV R1,@R5
ADD
MOV R7,@R4
DT R0
ADD #4,R5
ADD #4,R4
BF

FIG. 13

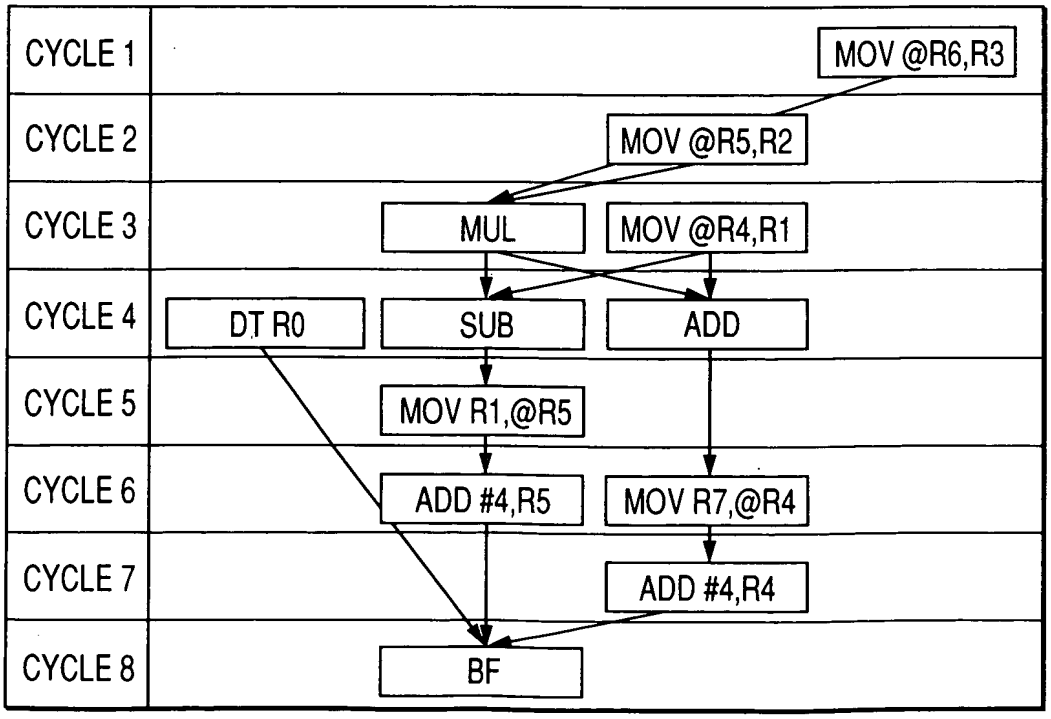

CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
CYCLE 5
CYCLE 6
CYCLE 7
CYCLE 8
MOV @R6,R3
MOV @R5,R2
MUL
MOV @R4,R1
DT R0
SUB
ADD
MOV R1,@R5
ADD #4,R5
MOV R7,@R4
ADD #4,R4
BF

FIG. 14

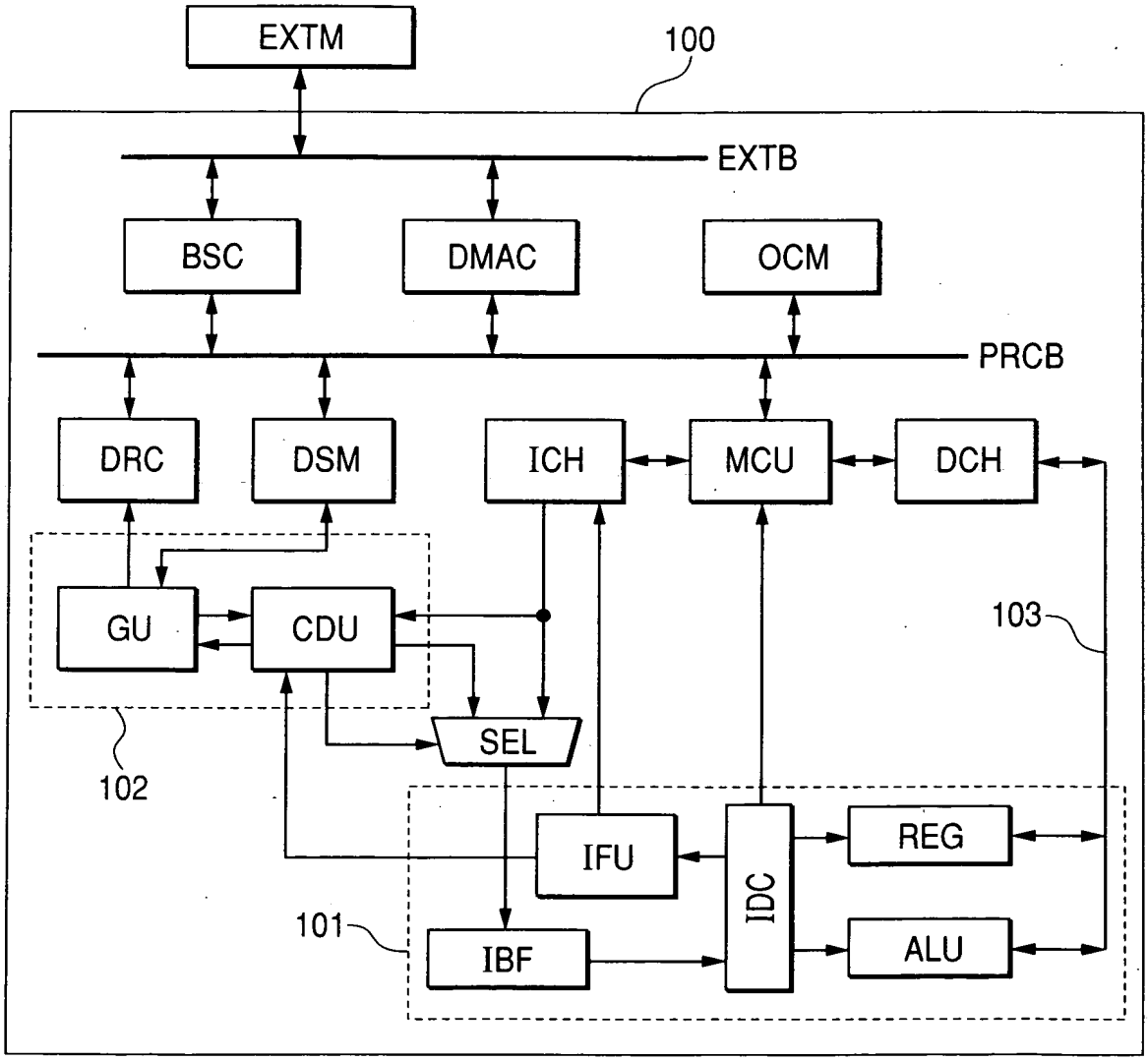
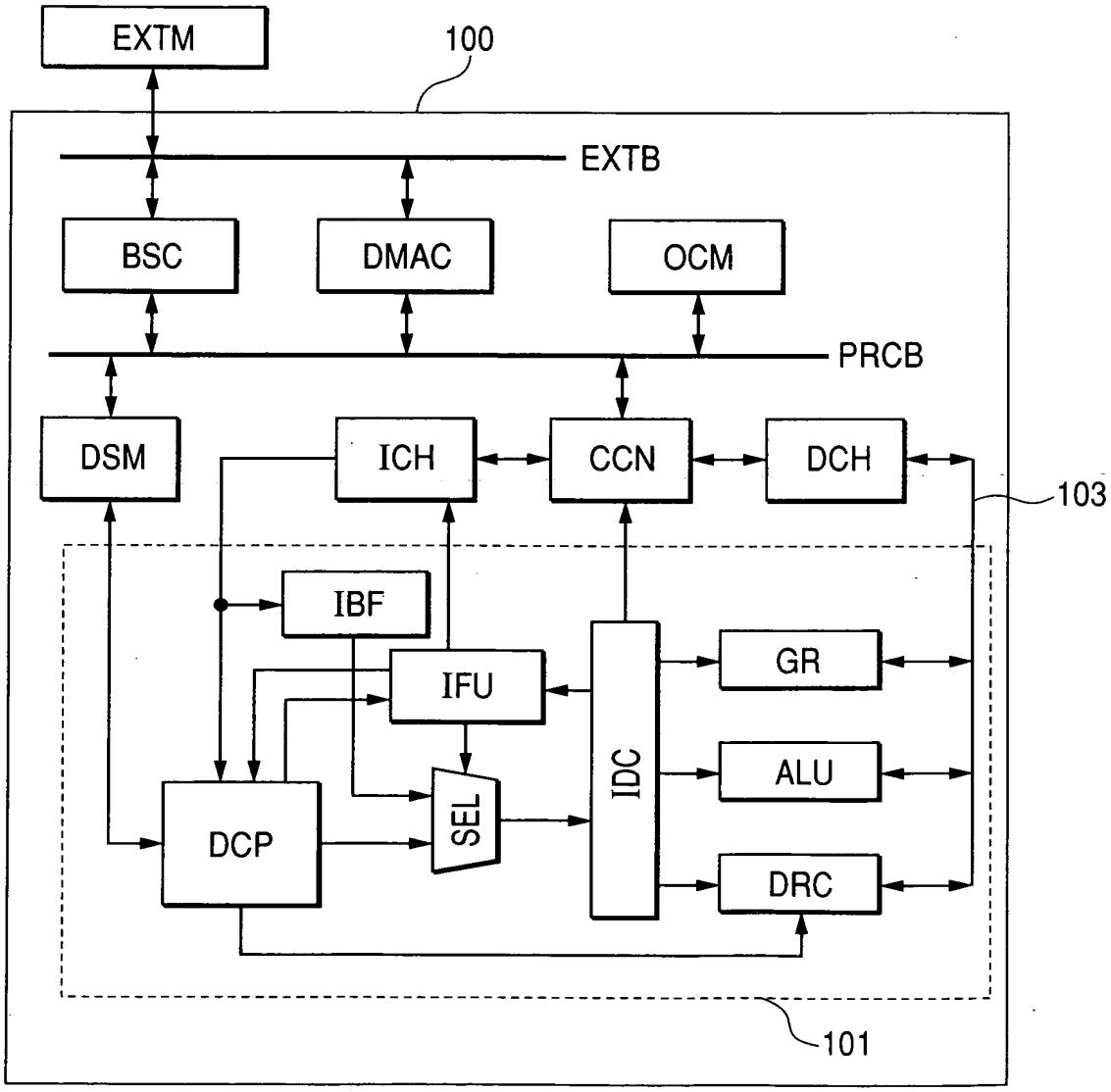

EXTM
100
EXTB
BSC
DMAC
OCM
PRCB
DRC
DSM
ICH
MCU
DCH
GU
CDU
103
SEL
102
IFU
IDC
REG
101
IBF
ALU

FIG. 15


EXTM
100
EXTB
BSC
DMAC
OCM
PRCB
DSM
ICH
CCN
DCH
103
IBF
IFU
GR
ALU
DRC
IDC
SEL
DCP
101